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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ESCHWEILER & ASSOCIATES LLC
629 EUCLID AVENUE, SUITE 1000
NATIONAL CITY BUILDING
CLEVELAND, OH 44114

EXAMINER	
PEREZ, JAMES M	
ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Docketing@eschweilerlaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/502,037	BACHER ET AL.	
	Examiner	Art Unit	
	JAMES M. PEREZ	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-9,12-16 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-9,12-16 and 20* is/are rejected.

7)☒ Claim(s) *10,11,17,18 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

This office action is responsive to the pre-brief appeal conference request and subsequent decision which was entered on 4/9/2009 and 6/26/2009 respectively. Thus the finality of the office action mailed on 1/9/2009 has been withdrawn.

Currently, claims 1 and 4-21 are pending.

Response to Arguments

1. Applicant's arguments, filed 3/9/2009, with respect to the claim rejections have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4-5, 14-16, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (herein referred to as AAPA) in view of Steudle (US 2002/0006119) further in view of Javerbring et al. (USPN 6,604,216).

With regards to claim 1, AAPA teaches an electronic transmitter device comprising a puncturing device, wherein the puncturing device (fig. 2: element P1: page 2, lines 12-32) comprises:

a first and a second intermediate data output (fig. 2: element P1: page 2, lines 12-32 and page 2a, Table 1: outputs of puncturing patterns for X and Y); wherein

the puncturing device is configured in such a way that it distributes an output data stream substantially uniformly in parallel between the first and second intermediate data outputs (fig. 2: element P1: page 2, lines 12-32 and page 2a, Table 1: wherein the puncturing pattern is substantially uniformly parallel between X and Y); and

wherein the puncturing device applies a puncture pattern (fig. 2: element P1: page 2, lines 12-32 and page 2a, Table 1), so that a number of bits of an input data stream corresponds, including the puncture locations, to a number of bits of the output data stream (fig. 2: element P1: page 2, lines 12-32 and page 2a, Table 1)

AAPA does not explicitly teach two Limitations: Limitation 1) a first and second data outputs are parallel; and Limitation 2) wherein said puncture locations are provided in the output stream as empty locations; and Limitation 3) wherein the puncturing device is further configured to output, in addition to the output data stream, a signal which indicates a position of an empty location in the output data stream.

Limitation 1)

Note that AAPA Table 1 teaches that the parallel punctured streams X and Y are applied to parallel/serial conversion (fig. 2: P1: page 2, lines 12-32 and page 2a, Table 1: "after parallel/serial conversion"). Immediately following the serial out of P1 the output data stream is applied to a serial to parallel converter (fig. 2: P1 and S/P).

One of ordinary skill in the art at the time of the invention would clearly understand that it would be obvious to modify puncturing element P1 in order to directly

output a first and second data output in parallel since a P/S conversion followed by a S/P conversion is functional equivalent to the Puncturing unit P1 directly outputting parallel data streams. Furthermore, one of ordinary skill in the art at the time of the invention would also clearly recognize the benefits of the modification described above since such a modification would obviously increase the processing efficiency of the system.

Limitation 2)

Steudle teaches creating empty (gaps) locations in an input signal using a puncturing device (paragraph 9: wherein the puncture locations are the empty locations) and are supplied to the rest of the transmitting device (paragraphs 8-9). Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to modify the known puncturing device disclosed in AAPA with the known method of gap insertion via puncturing as disclosed in Steudle in order to yield the predictable results and benefits of increased processing speed while maintaining the benefits of punctured convolutional code.

Limitation 3)

Javerbring teaches, "signaling of which puncturing pattern that has been used gives a large overhead...., [where no] flexible way of signaling which puncturing pattern P1, P2, ...Pn is used exists. Normally a number of predetermined puncturing schemes, i.e. bitmaps containing one's and zero's are applied, and which puncturing scheme is used is signaled to the receiver 120 in the subblock header" (col. 4, lines 5-18) (emphasis added).

One of ordinary skill in the art at the time of the invention would clearly recognize the advantages of a puncturing unit (in the transmitter) generating an additional signal which indicates a position of punctured data in the output data stream which signals puncturing protocol/pattern to the receiver, since signal the puncturing pattern enables the receiver to correctly de-puncture the transmitted signal thus preventing error due to improper de-puncturing protocols.

Therefore it would have been obvious to one of orindary skill in the art at the time of the invention modify the gap puncturing transmitter disclosed by AAPA in view of Steudle with the teachings of signaling puncturing pattern/protocol to the receiver disclosed by Javerbring since such a modification has the benefits of enabling the receiver to correctly de-puncturing the transmitted signal thus preventing error due to improper de-puncturing protocols.

With regards to claim 4, AAPA in view of Steudle further in view of Javerbring teaches the limitations such as the first and second data of claim 1.

AAPA teaches an interleaver arranged downstream of the puncturing device in a direction of the data streams (fig. 2: element P1 and 2: page 1, lines 1-11);

wherein a input of the of interleaver is directly or indirectly electrically connected to the first data output and the second data output of the puncturing device (fig. 2: element P1 and 2: page 1, lines 1-11),

AAPA does not explicitly teach the interleaver comprising: a first data input connected to the first data output of the puncturing device, and a second data input

connected to the second data output of the puncturing device.

One of ordinary skill in the art would clearly recognize the benefits of parallel processing over serial processing, since parallel processing decrease processing time of the receiver and lowers system complexity. Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to modify the interleaver and puncturing device of AAPA in order to implement the benefits of parallel processing which include decreased processing time and lower system complexity.

With regards to claim 5, AAPA in view of Steudle further in view of Javerbring teaches the limitations such as the first and second data of claim 4.

AAPA does not explicitly teach the interleaver comprises an n*m interleaver, n and m being natural numbers.

One of ordinary skill in the art at the time of the invention would clearly understand that the interleaver of AAPA obviously includes at least one subset of the claimed n*m interleaver wherein n and m being natural numbers greater than or equal to 1.

With regards to claim 14, AAPA in view of Steudle further in view of Javerbring teaches the limitations of claim 1.

AAPA teaches the puncturing device comprises a first puncturing element and a second puncturing element which is arranged downstream of the first puncturing element in the direction of the data stream (fig. 2: elements P1 and P2: page 2, lines 12-

32 and page 2, Table 2: ½ rate code).

AAPA does not explicitly teach puncturing device comprises one puncturing element.

One of ordinary skill in the art at the time of the invention would clearly understand that in the case wherein one of the puncturing elements had a puncturing pattern of all 1's (no puncturing), the disclosed system would implicitly have one puncturing element.

With regards to claim 15, AAPA in view of Steudle further in view of Javerbring teaches the limitations of claim 1.

AAPA teaches the puncturing device comprises a first puncturing element and a second puncturing element which is arranged downstream of the first puncturing element in the direction of the data stream (fig. 2: elements P1 and P2: page 2, lines 12-32).

With regards to claim 16, AAPA in view of Steudle further in view of Javerbring teaches the limitations of claim 1.

AAPA teaches the first puncturing element comprises a first and a second intermediate data output (fig. 2: element P1: page 2, lines 12-32 and page 2a, Table 1: outputs of puncturing patterns for X and Y), and is configured in such a way that it distributes an output data stream substantially uniformly in parallel between the first and second intermediate data outputs (fig. 2: element P1: page 2, lines 12-32 and page 2a,

Table 1: wherein the puncturing pattern is substantially uniformly parallel between X and Y); and

the second puncturing element comprises a first and a second data input (fig. 2: elements P2, X, and Y), the first data input of the second puncturing element being directly or indirectly electrically connected to the first data output of the first puncturing element (fig. 2: elements P2, X, and Y), and the second data input of the second puncturing element being directly or indirectly electrically connected to the first data output of the first puncturing element (fig. 2: elements P2, X, and Y).

AAPA does not explicitly teach the first and second data outputs are parallel;

Note that AAPA Table 1 teaches that the parallel punctured streams X and Y are applied to parallel/serial conversion (fig. 2: P1: page 2, lines 12-32 and page 2a, Table 1: "after parallel/serial conversion"). Immediately following the serial out of P1 the output data stream is applied to a serial to parallel converter (fig. 2: P1 and S/P).

One of ordinary skill in the art at the time of the invention would clearly understand that it would be obvious to modify puncturing element P1 in order directly output a first and second data output in parallel since a P/S conversion followed by a S/P conversion is functional equivalent to the Puncturing unit P1 directly outputting parallel data streams, while increasing the processing efficiency of the system.

With regards to claims 19-20, AAPA in view of Steudle further in view of Javerbring teaches the limitations of claim 15.

AAPA teaches the second puncturing element comprises a first and a second

intermediate data output (fig. 2: element P2: page 4: Table 2: outputs of puncturing patterns for X and Y), and is configured in such a way that it distributes an output data stream substantially uniformly in parallel between the first and second intermediate data outputs (fig. 2: element P2: page 4: Table 2: wherein the puncturing pattern is substantially uniformly parallel between X and Y); and

wherein the first and second intermediate data output is simultaneous and parallel (fig. 2: element P2: page 4: Table 2: outputs of puncturing patterns for X and Y)

AAPA does not explicitly teach the first and second data outputs are parallel;

Note that AAPA Table 2 teaches that the parallel punctured streams X and Y are applied to parallel/serial conversion (fig. 2: element P2: page 4: Table 2: "after parallel/serial conversion").

One of ordinary skill in the art would clearly recognize the benefits of parallel processing over serial processing, since parallel processing decrease processing time of the receiver and lowers system complexity. Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to modify the interleaver and puncturing device of AAPA in order to implement the benefits of parallel processing which include decreased processing time and lower system complexity.

4. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Steudle (US 2002/0006119) and Javerbring et al. (USPN 6,604,216) as applied to claim 5, further in view of Heichler (USPN 5,029,331).

With regards to claim 6, AAPA in view of Steudle further in view of Javerbring teaches the limitations such as the first and second data of claim 5.

AAPA does not explicitly teach the interleaver comprises a first shift register which is directly or indirectly electrically connected to its first data input, and a second shift register which is directly or indirectly electrically connected to its second data input.

Heichler teaches interleaver comprises a first shift register which is directly or indirectly electrically connected to its first data input (figs. 7-8: col. 4, line 55 through col. 5, line 38), and a second shift register which is directly or indirectly electrically connected to its second data input (figs. 7-8: col. 4, line 55 through col. 5, line 38).

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to modify the interleaver of AAPA in order to implement the benefits of parallel processing which include decreased processing time and lower system complexity.

With regards to claim 7, AAPA in view of Steudle further in view of Javerbring in further view of Heichler teaches the limitations such as the first and second data of claim 6.

AAPA does not explicitly teach wherein both shift registers are 8-bit shift registers.

Heichler teaches both shift registers are 8-bit shift registers (figs. 7-8: col. 4, line 55 through col. 5, line 38), wherein one of ordinary skill in the art at the time of the invention would clearly understand elastic FIFO (first-in first-out) memory can obviously be implemented as an 8-bit shift registers.

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to modify the interleaver of AAPA in order to implement the benefits of parallel processing which include decreased processing time and lower system complexity.

5. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Steudle (US 2002/0006119) and Javerbring et al. (USPN 6,604,216) with Heichler (USPN 5,029,331) as applied to claim 6, further in view of Ericsson (EP 1089440).

With regards to claim 8, AAPA in view of Steudle in further view of Javerbring with Heichler teaches the limitations of claim 6.

AAPA does not explicitly teach the interleaver comprises a matrix register.

Ericsson teaches the interleaver comprises a matrix register (figs. 3-4: paragraph 22).

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to modify the interleaver of AAPA with the interleaver of Ericsson in order to increase the system's tolerance to burst noise in the channel.

With regards to claim 9, AAPA in view of Steudle in further view of Javerbring with Heichler and Ericsson teaches the limitations of claim 8.

AAPA does not explicitly teach the interleaver comprises a matrix register.

Ericsson teaches the interleaver comprises a 16*18 matrix register (figs. 3-4: paragraphs 22 and 30-32)

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to modify the interleaver of AAPA with the interleaver of Ericsson in order to increase the system's tolerance to burst noise in the channel.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Steudle (US 2002/0006119) with Javerbring et al. (USPN 6,604,216) as applied to claim 4, further in view of Mead (US 2002/0003885).

With regards to claim 12, AAPA in view of Steudle further in view of Javerbring teaches the limitations of claim 4.

AAPA does not explicitly teach the interleaver comprises an RAM and is designed in such a way that the bit pairs which pass into the interleaver are written directly to predetermined RAM addresses.

Mead teaches interleaver comprises an RAM and is designed in such a way that the bit pairs which pass into the interleaver are written directly to predetermined RAM addresses (fig. 3: paragraph 13).

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to modify the interleaver of AAPA with the interleaver of Mead in order to

increase the processing speed of the interleaving device while maintaining the system's tolerance to burst noise in the channel via interleaving.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Steudle (US 2002/0006119) with Javerbring et al. (USPN 6,604,216) as applied to claim 4, further in view of Choi et al. (USPN 7,092,455).

With regards to claim 13, AAPA in view of Steudle further in view of Javerbring teaches the limitations of claim 4.

AAPA does not explicitly teach the interleaver is configured in such a way that, using the indication signal which is additionally transmitted by the puncturing device, the interleaver detects the empty locations in the parallel input data stream coming from the puncturing device, and does not include them in the further data processing.

Choi teaches a control signal indicative of the puncturing pattern for processing data signal at later stages (fig. 11: element 64: col. 8, line 43 through col. 9, line 5)

One of ordinary skill in the art at the time of the invention would clearly understand that it would be obvious for the interleaver to detect the empty locations in the parallel input data stream coming from the punching, and would thereby not include them in the further data processing since removing said empty locations would increase the throughput of the system while maintaining the benefits of high coding rates.

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to modify the interleaver of AAPA with the puncturing control signal of Choi in

order to increase the throughput of the system while maintaining the benefits of high coding rates.

Allowable Subject Matter

8. Claims 10-11, 17-18, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Peting (USPN 7,251,294) discloses outputs and symbol puncturing patterns for different code rates (col. 9, lines 1-58).

Ramesh (USPN 6,131,180) discloses convolutional encoding followed by a puncturing unit wherein the output out the puncturing unit is two parallel output steams (fig. 7: col. 6, lines 42-67: elements 92, 94, 96, 0_1 and 0_2).

Heichler et al. (USPN 5,029,331) discloses the use of parallel digital signal processing in convolutional encoders/decoders, interleavers/de-interleavers (i.e. data re-arranger) and puncturing/de-puncturing units (fig. 7).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES M. PEREZ whose telephone number is (571)270-3231. The examiner can normally be reached on Monday through Friday: 9am to 5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/James M Perez/
Examiner, Art Unit 2611
8/27/2009
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611